SCHEME OF EXAMINATION

FOR

MASTER OF TECHNOLOGY

[VLSI Design]

REGULAR PROGRAMME

Offered by

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGG.

Indira Gandhi Delhi Technical University for Women

(Established by Govt. of Delhi vide Act 09 of 2012)

(Formerly Indira Gandhi Institute of Technology)

Kashmere Gate Delhi-110006

M.Tech(VLSI Design)

FIRST SEMESTER

Paper Code	Paper Title	L	T/P	Credit
THEORY				
MVD-501	CMOS Analog Circuit Design	4	-	4
MVD-503	Digital Integrated Circuits	4	-	4
MVD-505	Hardware Description Languages	4	-	4
MVD-507	Semiconductor Devices	4	-	4
MVD-509	Advanced IC Processing	4	-	4
PRACTICALS				
MVD-511	CMOS Analog Circuit Design Lab	-	2	1
MVD-513	Digital Integrated Circuits Lab	-	2	1
MVD-515	Hardware Description Languages Lab	-	2	1
MVD-517	Technical Report Writing*	-	2	2
	TOTAL	**20**	**8**	**25**

*NUES (Non University Examination System)

SECOND SEMESTER

Paper Code	Paper Title	L	T/P	Credit
THEORY				
MVD-502	Device Modeling & Circuit simulation	4	-	4
MVD-504	VLSI subsystem design	4	-	4
MVD-506	Integrated Circuits for Analog Signal Processing	4	-	4
ELECTIVES (Choose any two)**				
MVD-508	Semiconductor Memory Design	4	-	4
MVD-510	Deep Submicron CMOS ICs	4	-	4
MVD-512	Optimization Techniques	4	-	4
MVD-514	Analog filter Design	4		4
MVD-516	Digital Techniques for High Speed Design	4	-	4
MVD-518	CMOS Mixed-Signal VLSI Design	4	-	4
MVD-520	Nanoelectronics: Devices and Materials	4	-	4
MVD-522	MEMS & Microsystems	4	-	4
PRACTICALS				
MVD-524	Device Modeling & Circuit simulation Lab	-	2	1
MVD-526	VLSI subsystem design Lab	-	2	1
MVD-528	Lab based on elective(s)	-	2	1

MVD-530	Term Paper*	-	2	2
	TOTAL	**20**	**8**	**25**

THIRD SEMESTER

Paper Code	**Paper Title**	**L**	**T/P**	**Credit**
THEORY				
MVD-601	Low power VLSI Design	4	-	4
MVD-603	ASIC Design	4	-	4
ELECTIVES(Choose any one)**				
MVD-605	VLSI Interconnects	4	-	4
MVD-607	VLSI design Algorithms	4	-	4
MVD-609	VLSI Design Verification and Test	4	-	4
MVD-611	RF Integrated Circuits	4	-	4
PRACTICALS				
MVD-613	Low power VLSI Design Lab	-	2	1
MVD-615	ASIC Design Lab	-	2	1
MVD-617	Minor Project	-	8	12
	TOTAL	**12**	**12**	**26**

FOURTH SEMESTER

Paper Code	**Paper Title**	**L**	**T/P**	**Credit**
MVD -602	Dissertation	-	30	24
MVD -604	Seminar and Progress Report*	-	04	04
	TOTAL		**34**	**28**

*NUES (Non University Examination System)
**Any of the subject may be chosen in distance learning mode such as Massive Open Online Courses(MOOCs etc) and supervised by internal faculty-in-charge.

1. The total number of credits of the M. Tech Programme. = 104.
2. Each student shall be required to appear for examination in all courses. However, for the award of the degree a student shall be required to earn a minimum of 100.

Paper Code: MVD-501 **L T C**
Paper Title: CMOS Analog Circuit Design **4 0 4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

Introduction to MOSFET device structure and operation, MOS as amplifier, Biasing in MOS amplifier circuits, small signal equivalent circuit model, Single stage MOS amplifiers, characterizing amplifiers, MOS internal capacitance and high frequency model, frequency response (10Hrs)

UNIT 2

IC biasing-current sources, current mirrors and current-steering circuits, cascode and wilson current mirror, Common Source, common gate and common drain IC amplifiers, low frequency and high frequency response, noise performance, Multiple-Transistor IC amplifiers, Cascode configuration, folded cascode and self cascode structure, Voltage follower, flipped voltage follower

(10Hrs)

UNIT 3

MOS differential pair, small signal operation, differential gain ,common mode gain, common mode rejection ration, non ideal characteristics, active loaded differential amplifier, Frequency response, Noise Spectrum, sources, types, Thermal and Flicker noise, representation in circuits, Noise bandwidth, Noise figure (10Hrs)

UNIT 4

General feedback structure, negative feedback, four basic topologies, loop gain, stability, effect of feedback on amplifier poles, single pole response, two pole response, Frequency compensation, Compensation Techniques, Pole splitting (10Hrs)

References:

1. Sedra and Smith, "Microelectronic circuits", 5th Edition, Oxford University press, 2005.
2. Kenneth R. Laker and Willy M.C. Sansen, "Design of Analog Integrated Circuits and systems", 2nd Edition, McGraw-hill, 1994.
3. Philip E. Allen & Douglas R. Holberg, "CMOS Analog Circuit Design", 2nd Edition, Oxford University Press, 2002.
4. Behzad Razavi, "Design of Analog CMOS Integrated Circuit", 3rd Edition, Tata McGraw Hill, 2003.
5. Gray R.Paul, Hurst J. Paul, Lewis H. Stephen and Meyer G. Robert, "Analysis and Design of Analog Integrated Circuits", 4th Edition, John Wiley and Sons, 2004.

Paper Code: MVD-503 **L T C**
Paper Title: Digital Integrated Circuits **4 0 4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

MOS transistor as switch, CMOS inverter, static behavior, switching threshold, noise margins, dynamic behavior, propagation delay, CMOS inverter power consumption, static and dynamic power, energy-delay analysis, technology scaling and its impact on inverter metrics (10Hrs)

UNIT 2

Static CMOS logic, Pseudo-NMOS logic, pass transistors, complementary pass logic, CMOS transmission-gate logic, differential CMOS logic, transistor sizing, Logical effort, dynamic CMOS logic, dynamic CMOS circuit techniques, high performance dynamic CMOS circuits, charge sharing, design and implementation of Combinational CMOS circuits (10Hrs)

UNIT 3

Sequential MOS logic circuits, timing metrics for sequential circuits, bistability principle, static latches and flip flops, CMOS edge triggered FFs, registers, ratioed and ratioless logic, dynamic latches and registers, pipelining, optimization of sequential circuits, Nonbistable sequential circuits, Schmitt trigger (10Hrs)

UNIT 4

Timing issues in digital circuits, timing classification, choosing a clocking strategy, sources of skew and jitter, clock distribution techniques, self timed circuit, synchronizers and arbiters, distributed clocking, Introduction to BiCMOS and GaAs logic family (10Hrs)

References:

1. Jan M. Rabaey, Anantha chandrakasan, Borivoje nikolic, "Digital Integrated Circuits-A design perspective", 2nd Edition, Pearson, 2010.
2. Sung Ms Kang, Yusuf Lablebici, "CMOS Digital Integrated Circuits Analysis & Design", 3rd Edition, Tata Mc-Graw Hill, 2003.
3. Ken Martin, "Digital Integrated Circuit Design", 1st Edition, Oxford University Press, 2004.

Paper Code: MVD-505 **L T C**
Paper Title: Hardware Description Languages **4 0 4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

Introduction to VHDL, behavioral, data flow, structural models, simulation cycles, process, concurrent & sequential statements, loops, delay models, library, packages, functions, procedures, test bench, design of digital circuits using VHDL (10 Hrs)

UNIT 2

Introduction to Verilog HDL, hierarchical modeling concepts, Lexical conventions, data types, system tasks and compiler directives, modulus and ports, variable, arrays, tables, operators, expressions, signal assignments, nets, registers, concurrent & sequential constructs, tasks & functions (10Hrs)

UNIT 3

Gate-level, Dataflow and behavioral modeling using Verilog HDL, advanced Verilog topics, timing and delays, delay models, path delay modeling, timing checks, switch level modeling, user defined primitives, programming language interface (10Hrs)

UNIT 4

Logic Synthesis with hardware description language, impact of logic synthesis, synthesis design flow, RTL description, technology mapping and optimization, technology library, design constraints Introduction to SystemVerilog, verification techniques (10Hrs)

References:

1. Peter J Ashenden, "The Designer's Guide to VHDL", 2nd Edition, Morgan Kaufmann Publishers, 2002.
2. Stefan Sjoholm & Lennart Lindth, "VHDL for Designers", 1st Edition, Prentice Hall, 2002.
3. J. Bhaskar, "Verilog HDL Synthesis - A Practical Primer", 3rd Edition, Star Galaxy Publishing, 2008.
4. S. Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", 2nd Edition, Prentice Hall, 2006.

5. Mintz**,** Mike, Ekendahl**,** Robert, "Hardware Verification with System Verilog: An Object-Oriented Framework", 1st Edition, Springer, 2010.

Paper Code: MVD-507	**L**	**T**	**C**
Paper Title: Semiconductor Devices	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

Elemental and compound semiconductors, narrow & wide energy gap semiconductors, direct & indirect semiconductors, choice of semiconductors for specific applications, review of semiconductor fundamentals, energy band, Carrier transport phenomena, Recombination and generation, surface effects, traps (10Hrs)

UNIT 2

PN junction, Schottky junctions, Ohmic contacts, BJT device Design, nonideal effects, frequency limitations, MOSFET Operation, subthreshold conduction, mobility variation, velocity saturation threshold voltage modifications, threshold adjustment by Ion implantation, Lightly doped drain MOS transistor, breakdown voltage, radiations and hot electron effects (10Hrs)

UNIT 3

Introduction to modern VLSI Devices, Polysilicon emitter transistors, Heterojunctions, 2D electron gas, band alignment, SOI MOSFETs, PDSOI, FDSOI, Source/drain engineering, Brief introduction to HEMTs, MESFET(Metal semiconductor FET) and MODFET(Modulation doped FET). (10Hrs)

UNIT 4

New VLSI device structures, from bulk to SOI to multi-gate, double gate MOSFET, FinFET, SiGe technology, strain influence on electron mobility, strain enhanced Si based transistors, strained Si CMOS, SiGe HBTs, SiGe MODFETs, Nanowires (10Hrs)

References:

1. Donald A. Neamen, "Semiconductor Physics and devices", 3rd Edition, Tata McGraw Hill, 2008.

2. Taur and Ning, "Fundamentals of Modern VLSI Devices",2nd Edition, Cambridge Press, 2002.
3. Ben G. Streetman & S. Banerjee, "Solid state electronic devices", 6th Edition, Prentice Hall, 2010.

Paper Code: MVD-509	**L**	**T**	**C**
Paper Title: Advanced IC Processing	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

Overview of modern CMOS technology, Substrate selection, active region formation, device isolation, well formation, gate and source/drain formation, contact and local interconnects, multilevel metal formation, comparison between bulk and SOI CMOS technologies (10Hrs)

UNIT 2

Crystal growth, crystal structure, crystal defects, raw materials and purification, electronic grade silicon, Czochralski and float-zone crystal growth methods, Wafer preparation and specifications, SOI wafer manufacturing clean rooms, wafer cleaning and gettering, Basic concepts, manufacturing methods and equipment, Measurement methods (10Hrs)

UNIT 3

Photolithography, Light sources, Photoresists, Wet and Dry oxidation, growth kinetics, Diffusion, fick's laws, Ion implantation, Chemical and physical vapour deposition, epitaxial growth, deposition of dielectrics and metals commonly used in VLSI, Wet etching, Plasma etching, Etching of materials used in VLSI, Contacts, Vias, Multi-level Interconnects, Silicided gates and S/D regions, Reflow & planarization (10Hrs)

UNIT 4

Functions of packaging, rent's Rule, packaging techniques, through hole, surface mount, types of single chip packaging, bond wire, flip chip technology, tape automated Bonding, Thermal Management, Interconnection topology, Introduction to system packaging, System-in-package, Multi-Chip Module, 3D Packaging, Future Trends (10Hrs)

References:

1. James D. Plummer,M.D.Deal and P.B.Griffin, "Silicon VLSI Technology, Fundamentals, Practice and Modeling", 1st Edition, Pearson education, 2007.
2. Sorab Ghandhi, "VLSI Fabrication Principles",2nd Edition, John Wiley and Sons, 2008.
3. S.M.Sze, "VLSI Technology",2nd Edition, McGraw-Hill, 2002.
4. H. B. Bakoglu**,** "Circuits, Interconnections, and Packaging for VLSI**",** 1st Edition, Addison Wesley Longman Publishing, 1990.

Code No: MVD -511	**L**	**P**	**C**
Lab : CMOS Analog Circuit Design Lab	**-**	**2**	**1**

Experiments will be based on CMOS Analog Circuit Design Theory course

Code No: MVD -513	**L**	**P**	**C**
Lab : Digital Integrated Circuits Lab	**-**	**2**	**1**

Experiments will be based on Digital Integrated Circuits Theory course

Code No: MVD -515	**L**	**P**	**C**
Lab : Hardware Description Languages Lab	**-**	**2**	**1**

Experiments will be based on Hardware Description Languages Theory course

Code No: MVD -517	**L**	**P**	**C**
Technical Report Writing	**-**	**2**	**2**

Technical reports describe the progress or results of scientific or technical research and development. The purpose of a technical report is to completely and clearly describe technical work, why it was done, results obtained and implications of those results. Technical reports present facts and conclusions about the designs and other projects. Typically, a technical report includes research about technical concepts as well as graphical depictions of designs and data. For guidelines of technical report writing, following website may be referred.
www.theiet.org/students/resources/technicalreport.cfm

Paper Code: MVD-502	**L**	**T**	**C**
Paper Title: Device Modeling & Circuit simulation	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks: 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

Overview of MOS transistor physics, Two-Terminal MOS structure, Flat -band voltage, Effect of Gate-substrate voltage on surface condition, Inversion, Small signal capacitance, Three-Terminal MOS structure, Body effect, regions of inversion, Pinch-off voltage, Four Terminal MOS Transistor, regions of inversion, charge sheet model, interpolation model, body referenced model (10Hrs)

UNIT 2

MOS transistor large-signal modeling, quasi-static operation, limitations of quasi-static model, introduction to non-quasi static model, MOS transistor small-signal modeling, low & medium frequency model, high frequency model, considerations in MOS modeling for RF applications, gate resistance, transition frequency, maximum frequency of oscillation, Noise model (10Hrs)

UNIT 3

MOSFET modeling for circuit simulation, Types of models, system for data acquisition and parameter extraction, properties of good models, Introduction to SPICE modeling, modeling of resistor, capacitor, inductor, diode, BJT, JFET, MOSFET, model parameters, Brief overview of BSIM and EKV model , Device and process simulator (10Hrs)

UNIT 4

Circuit simulation techniques, DC analysis, AC analysis, transient analysis, SPICE Modeling of Process Variation, Process corners, Monte Carlo simulation, and sensitivity/worst case analysis, Simulation of digital and analog circuits, transfer function, frequency response, Noise analysis, distortion and spectral analysis (10Hrs)

References:

1. Y. Tsividis, "Operation and modeling of MOS transistors",2nd Edition, McGraw-Hill, 1999.
2. Paul W. Tuinenga, "SPICE: A Guide to Circuit Simulation and Analysis Using PSpice", 3rd Edition, Pearson, 2006.
3. Paolo Antognetti and Giuseppe Massobrio, "Semiconductor Device Modeling with SPICE", 2nd Edition, Tata McGraw-Hill, 2010.
4. BSIM Model (http://www-device.eecs.berkeley.edu/bsim/)

5. EKV Model (http://ekv.epfl.ch/)

Paper Code: MVD-504	**L**	**T**	**C**
Paper Title: VLSI subsystem design	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

Moore's Law, technology node, ITRS, VLSI and systems, cost of design, types of chips, specialized standard parts, ASICs, System-on-Chips(SoCs), IC design techniques, Hierarchical Design, Design Abstraction, Computer-Aided Design, IC design flow, Transistors and layout, Wires and Vias, Design Rules, Layout Tools (10Hrs)

UNIT 2

Chips and their subsystems, Combinational Shifter, Adder, ALU, Multiplier, high density Memory, Image sensor, FPGA, Programmable logic array, Buses and Networks-on-Chips, Data Paths, , Subsystem optimization, Pipelining (10Hrs)

UNIT 3

Intellectual property (IP)-based design, IP types, IP Across the Design Hierarchy, The IP Life Cycle, Creating IP, Using IP, VLSI subsystems as IP, Systems-on-chips and embedded CPUs, Multiprocessor System-on-Chip Design (10Hrs)

UNIT 4

Chip-level layout, floorplanning methods, Block Placement, Channel Definition, Global Routing, Switchbox Routing, Global Interconnect, Interconnect Properties and Wiring Plans, Power Distribution, Clock Distribution, Floorplan Design, Design Validation, Off-Chip Connections, I/O Architecture (10Hrs)

References:

1. Wayne Wolf, "Modern VLSI design: IP-Based Design", 4th Edition, Pearson, 2008.
2. Wayne Wolf, "Modern VLSI design: System-on-Chip Design", 3rd Edition, Pearson, 2002.
3. Jacob Backer, Harry W. Li and David E. Boyce, "CMOS Circuit Design, Layout and Simulation",3rd Edition, Prentice Hall of India, 2010.

4. Dan Clein, "CMOS IC Layout: Concepts, Methodologies and Tools",1st Edition, Newnes Elsevier, 1999.

Paper Code: MVD-506	**L**	**T**	**C**
Paper Title: Integrated Circuits for Analog Signal Processing	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

Signals, Information, Interference and noise, signal classification, dynamic range, S/N ratio, Functions in analog signal processing, linear non linear fuctions, impedance adaptation, amplitude and level matching, terminal matching, buffering filtering, linearization, domain conversions, errors in analog signal processing (10Hrs)

UNIT 2

Voltage amplification, practical voltage amplifiers, effects of finite input impedances, building blocks for voltage amplifiers, Current to voltage and voltage to current conversion, current integrators, mirrors, amplifiers, conveyors (10Hrs)

UNIT 3

CMOS analog integrated circuits, analog building blocks, Op-amp design, practical opamp characteristics and model, DC offset and DC bias currents, Gain, bandwidth and slew rate, Noise, Input stage, output stage, CMOS OTA, ideal model, OTA building block circuits, design of simple OTA (10Hrs)

UNIT 4

Signal rectifications, AC/DC conversion, CMOS implementation of adder, subtractor, squarer, analog multiplier, analog dividers, differentiator and integrator circuits, Impedance transformation and conversion, Analog multiplexers (10Hrs)

References:

1. Pallas Areny and John G.Webster, "Analog Signal Processing",1st Edition, John wiley, 1999.
2. Tlelo-Cuautle and Esteban, "Integrated Circuits for Analog Signal Processing", 1st Edition, Springer, 2013.
3. Ismail, Mohammed and Sawan, Mohamad,"Analog Circuits and Signal Processing" The Springer International Series in Engineering and Computer Science, 2012.

4. M.Ismail and T. Fiez, "Analog VLSI signal and Information processing",2nd Edition, Mc-Graw hill, 2000.

Paper Code: MVD-508	**L**	**T**	**C**
Paper Title: Semiconductor Memory design	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

MOS RAM technologies, SRAMs, architecture, SRAM cell and peripheral, Circuit operation, SRAM Technologies, SOI Technology, advanced SRAM architectures and technologies, DRAM technology development, CMOS DRAMs cell, theory and advanced cell structures (10Hrs)

UNIT 2

Nonvolatile memories, MOS ROMs, PROMs, EPROMs, One-Time Programmable EPROMS, Electrically erasable PROMs, EEPROM technology and architecture, Nonvolatile SRAM-Flash Memories, advanced Flash Memory architecture (10Hrs)

UNIT 3

Memory failure modes, reliability modeling, Prediction design for reliability, reliability test structures, reliability screening and qualification, radiation effects, radiation hardening, process and techniques, Radiation hardened memory characteristics, soft errors (10Hrs)

UNIT 4

Ferroelectric random access memories (FRAMs), Gallium arsenide FRAMs, Analog memories, Magneto resistive RAMs, Experimental memory devices, Memory hybrids and MCMs (2D), Memory stacks and MCMs(3D), memory cards, high density memory packaging (10Hrs)

References:

1. Ashok K. Sharma, "Advanced Semiconductor Memories: Architectures, Designs, and Applications", 2nd Edition, John Wiley, 2009.
2. A.K Sharma, "Semiconductor Memories Technology, Testing and Reliability",1st Edition IEEE Press, 2003.
3. Luecke Mize Care, "Semiconductor Memory design & application", 1st Edition, Mc-Graw Hill, 1999.

4. Belty Prince, " Semiconductor Memory Design Handbook" , 1st Edition, IEEE Computer Society, 2001.

Paper Code: MVD-510	**L**	**T**	**C**
Paper Title: Deep Submicron CMOS ICs	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

MOS scaling, classification, DSM (Deep submicron) effects on devices, physical and geometrical effects on the behavior of MOS transistor, carrier mobility, channel length modulation, short channel, narrow channel effects, drain feedback, hot carrier effects (10Hrs)

UNIT 2

MOS transistor leakage mechanisms, weak inversion behavior, gate oxide tunneling, reverse-bias junction leakage, gate induced drain leakage, Impact ionization, overall leakage interactions and considerations (10Hrs)

UNIT 3

Signal integrity, cross talk and signal propagation, power integrity, supply and ground bounce, substrate bounce, EMC, soft errors, Variability, spatial and time based variations, global and local variations, transistor matching, parameter, process corners, causes for variations (10Hrs)

UNIT 4

Deep submicron IC reliability, punch through, electromigration, hot carrier degradation, negative bias temperature instability, Latch-up, Electro-static discharge, charge injection during fabrication process, Effects of scaling on MOS IC design and consequences for the technology roadmap for Semiconductors (10Hrs)

References:

1. Harry Veendrick, "Deep-Submicron CMOS ICs", 2nd Edition, Kluwer Academic publishers,2000.
2. John Paul Uyemura, "Chip Design for Submicron VLSI", 2nd Edition., Thomson, 2006.
3. Wolfgang nebel and Jean mermet, "Low power design in deep submicron electronics", NATO ASI series, Kluwer Academic publishers, 2012.

Paper Code: MVD-512 **L T C**
Paper Title: Optimization Techniques **4 0 4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

Statistical modeling, sources of variations, Monte Carlo techniques, Process variation modeling-Pelgrom's model, Principal component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models, Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation (10Hrs)

UNIT 2

Convex optimization**,** Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Posynomial fitting (10Hrs)

UNIT 3

Genetic algorithm introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement,routing technology,Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multiway Partitioning Hybrid genetic-encoding-local improvement-WDFRComparison of Cas-Standard cell placement-GASP algorithm-unified algorithm (10Hrs)

UNIT 4

GA routing procedures and power estimation, Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm. (10Hrs)

References:

1. Ashish Srivastava, Dennis Sylvester, David Blaauw "Statistical Analysis and Optimization for VLSI:Timing and Power" ,2nd Edition, Springer, 2005.
2. Pinaki Mazumder, E.Mrudnick, "Genetic Algorithm for VLSI Design,Layout and test Automation",2nd Edition, Prentice Hall,2000.

3. Stephen Boyd, Lieven Vandenberghe "Convex Optimization", 1st Edition, Cambridge University Press, 2004.
4. Behzad Razavi, "Design of Analog CMOS Integrated Circuit",1st Edition, McGraw Hill, 2003.

Paper Code: MVD-514	**L**	**T**	**C**
Paper Title: Analog Filter Design	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

Monolithic filters, digital filters, analog discrete-time filters, analog continous-time filters, Introduction to analog filters, CMOS filters descriptive terminology, filter transmission, types and specifications, Filter transfer function, relationship among the time domain, frequency domain, s domain (10Hrs)

UNIT 2

Active and passive filter synthesis. Standard low-pass approximations, Butterworth, Chebyshev, Inverse Chebyshev, Cauer, Bessel, Elliptical, frequency transformations, First-order and Second order filter functions, Active filters, inductor based filter, two integrator loop topology (10Hrs)

UNIT 3

Switched capacitor filters, Basic principle and practical circuits, continuous type filters MOSFET-C, OTA-C filters, implementation techniques towards low power supply voltages and low distortion, frequency and time domain relationship, pole and zero locations (10Hrs)

UNIT 4

Filter synthesis for very high frequencies, synthesis methods, biquads, gyrators, Generalized immittance converter (GIC), inductor simulation using GIC, Introduction to Log-domain filters, Analog adaptive filters, Low voltage Analog filters in nanometer CMOS (10Hrs)

References:

1. M. E. Van Valkenburg and Mac Elwyn Van Valkenburg, "Analog Filter Design" 1st Edition,Oxford University Press, 2000.

2. Lawrence P. Huelsman, "Active and passive analog filter design: an introduction, Volume 1", 1st Edition, McGraw-Hill, 1993.
3. Larry D. Paarmann, "Design and Analysis of Analog Filters: A Signal Processing Perspective", 1st Edition, Kluwer Academic Publishers, 2001.

Paper Code: MVD-516	**L**	**T**	**C**
Paper Title: Digital Techniques for High Speed Design	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

Trends in High-Speed Design, backplane configurations, SerDes technology, Signal integrity, Signaling technologies and devices, Gunning transceiver Logic, Low voltage differential signaling(LVDS), Bus LVDS, LVDS multipoint, High-speed transceiver logic and Stub-series terminated logic, ECL, Current-mode logic, FPGAs - 3.125 Gbps rocket IOs and Hard copy devices, Fiber optic components, High speed interconnects and cabling (10Hrs)

UNIT 2

Memory device overview, memory signaling technologies, double data rate SDRAM (DDR, DDR2), GDDR3, ZBT, FCRAM, SigmaRAM, RLDRAM, DDR SRAM, Flash, FeRAM, and MRAM, Quad data rate SRAM, Direct Rambus DRAM(DRDRAM), Xtreme data rate DRAM, FlexPhase and ODR (10Hrs)

UNIT 3

Differential and mixed-mode S parameters, Time domain reflectometry(TDR), Time domain transmission(TDT) and VNAs, Modeling with IBIS, Overview of EDA Tools for high-speed design, simulation, verification and layout (10Hrs)

UNIT 4

Advances in design, Modeling, Simulation and measurement validation of high performance Board-to-Board 5-to-10 Gbps Interconnects, High-Speed Fiber-Optic transceivers, SerDes transceivers, serializers and deserializers, WarpLink SerDes system, Emerging protocols and technologies, Electrical Optical Circuit Board, Rapid IO, PCI Express and express card (10Hrs)

References:

1. Tom Granberg, "Handbook of Digital Techniques for High-Speed Design", 1st Edition, Prentice hall, 2012.
2. Howard Johnson and Martin Graham, "High Speed Digital Design: A Handbook of Black Magic", 2nd Edition, Prentice Hall, 2000.

Paper Code: MVD -518	**L**	**T**	**C**
Paper Title: CMOS Mixed-Signal VLSI Design	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

Analog and discrete-time signal processing, analog integrated continuous-time and discrete-time filters, Analog continuous-time filters, passive and active filters, basics of analog discrete-time filters and Z-transform (10Hrs)

UNIT 2

Switched-capacitor filters, Nonidealities in switched-capacitor filters, switched capacitor filter architectures, switched capacitor filter applications, Basics of data converters, Successive approximation ADCs, Dual slope ADCs, Flash ADC, Pipeline ADC (10Hrs)

UNIT 3

Hybrid ADC structures, high resolution ADC, DAC, Mixed signal layout, Interconnects and data transmission, Voltage-mode signaling and data transmission, Current-mode signaling and data transmission. (10Hrs)

UNIT 4

Introduction to frequency synthesizers and synchronization, basics of (Phase Locked Loop)PLL, PLL implementation techniques, Digital and Analog PLL, performance parameters, Delay Locked Loop(DLL), characteristics, advantages over PLL, implementation techniques (10Hrs)

References:

1. R. Jacob Baker, "CMOS mixed-signal circuit design", 2nd Edition, John Wiley, 2009.
2. Behad Razavi, "Design of analog CMOS integrated circuits", McGraw-Hill, 2003.
3. R. Jacob Baker, "CMOS circuit design, layout and simulation" 2nd Edition, IEEE press, 2008.

Paper Code: MVD -520	**L**	**T**	**C**
Paper Title: Nanoelectronics: Devices and Materials	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

Nano devices, materials and characterization, technology node, Basic CMOS Process flow, MOS scaling theory, Issues in scaling MOS transistors, Short channel effects, description of a typical 65 nm CMOS technology, requirements for non classical MOS transistor (10Hrs)

UNIT 2

MOS capacitor, interface quality, Gate oxide thickness, scaling trend, Interface states, bulk charge, band offset, stability, reliability, C-V and I-V techniques, Metal gate transistor, requirements and integration issues, transport in Nano MOSFET, velocity saturation, ballistic transport, injection velocity, velocity overshoot, SOI, PDSOI and FDSOI, FinFET, surround gate FET (10Hrs)

UNIT 3

Schotky junctions on Silicon, Germanium, work function pinning, strain, channel quantization, Compound semiconductors material properties, MESFETs, Hetero structure MOSFETs exploiting novel materials, strain, quantization, Synthesis of nanomaterials, CVD, Nucleation and growth, ALD, Epitaxy, MBE (10Hrs)

UNIT 4

Heterostructure growth and characterization, Quantum wells, thickness measurement, Contact step height, Optical reflectance, ellipsometry, characterization techniques for nanomaterials, applications and interpretation of results, emerging nano materials, Nanotubes, nanorods and other nano structures, LB technique, Soft lithography, Microwave assisted synthesis, Self assembly (10Hrs)

References:

1. Anupama B. Kaul, "Microelectronics to Nanoelectronics: Materials, Devices & Manufacturability",1st Edition, Taylor francis, 2013.
2. Byung-Gook Park,Sung Woo Hwang, Young June Park, " Nanoelectronic Devices", 1st Edition,Pan Stanford publishing, 2012.
3. Wolfgang Fahrner, "Nanotechnology and Nanoelectronics: Materials, Devices, Measurement Techniques", 1st Edition, Springer, 2005.

Paper Code: MVD -522	**L**	**T**	**C**
Paper Title: MEMS & Microsystems	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

Introduction to MEMS & Microsystems, Introduction to Microsensors, Evaluation of MEMS, Microsensors, Market survey, application of MEMS, MEMS Materials, MEMS materials properties, microelectronic technology for MEMS, micromachining technology for MEMS (10Hrs)

UNIT 2

Micromachining process, Etch stop techniques and microstructure, surface and quartz Micromachining, Fabrication of micromachined microstructure, Microstereolithography MEMS microsensors, thermal micromachined microsensors, Mechanical MEMS, Pressure and flow sensor, Micromachined flow sensors, MEMS inertial sensors (10Hrs)

UNIT 3

Micromachined microaccelerometers for MEMS, MEMS accelerometers for avionics, Temperature drift and damping analysis, Piezoresistive accelerometer technology, MEMS capacitive accelerometer, MEMS capacitive accelerometer process (10Hrs)

UNIT 4

MEMS gyro sensor, MEMS for space application, Polymer MEMS & carbon nano tubes(CNT), Wafer bonding & packaging of MEMS, Interface electronics for MEMS, MEMS for biomedical applications (Bio-MEMS) (10Hrs)

References:

1. Tai-Ran Hsu, "MEMS and Microsystems: Design and Manufacture", 1st Edition, McGraw-Hill, 2002.
2. Ghodssi, Reza; Lin, Pinyen, "MEMS Materials and Processes Handbook", 1st Edition, Springer, 2011.
3. Mohamed Gad-el-Hak, "MEMS: Introduction and Fundamentals", 1st Edition, Taylor and Francis, 2006.
4. Jan Korvink and Oliver Paul, "MEMS: A Practical Guide to Design, Analysis and Applications",1st Edition, Springer, 2006.

Code No: MVD -524	**L**	**P**	**C**
Lab : Device Modeling & Circuit simulation Lab	**-**	**2**	**1**

Experiments will be based on Device Modeling & Circuit simulation Theory course

Code No: MVD -526	**L**	**P**	**C**
Lab : VLSI Subsystem design Lab	**-**	**2**	**1**

Experiments will be based on VLSI Subsystem design Theory course

Code No: MVD -528	**L**	**P**	**C**
Lab : Lab based on elective(s)	**-**	**2**	**1**

Experiments will be based on based on elective(s)

Code No: MVD -530	**L**	**P**	**C**
Term Paper	**-**	**2**	**2**

Term papers are generally intended to describe an event, a concept or argue a point. The topic for the term paper may be based on the recent trends in technology/Industry or Academia research outcomes. The guidelines for writing are same as that for technical report writing.

Paper Code: MVD-601 **L T C**
Paper Title: Low power VLSI Design **4 0 4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

Introduction, battery technology summary, sources of CMOS power consumption, need for low power VLSI chips, dynamic power, static power, switching power, computing power versus chip power, SOI and Bulk technology (10Hrs)

UNIT 2

Impact of technology Scaling - Technology and Device, transistor sizing, gate oxide thickness, Technology options for low power, design options for power reduction, architectural level approaches, voltage scaling, power management, Circuit level approaches, Low power digital cells library (10Hrs)

UNIT 3

Low power Analog integrated circuits, challenges in low voltage analog circuit design, issues about low power supply voltage. Basic building blocks in analog design, cascode structure, self cascode structure, voltage follower, flipped voltage follower (10Hrs)

UNIT 4

Low voltage analog circuit design techniques, roadmap, design of analog circuits using low voltage implementation techniques, classification of body bias techniques, Dynamic Threshold MOSFET, Bulk driven technique, Floating Gate MOSFET, subthreshold analog circuits (10Hrs)

References:

1. Gary K. Yeap, Farid N. Najm, "Low power VLSI design and technology", 1st Edition, World Scientific Publishing Ltd.,2004.
2. Rabaey, Pedram, "Low power design methodologies", 2nd Edition, Kluwer Academic, 2004.
3. Kaushik Roy, Sharat Prasad,"Low-Power CMOS VLSI Circuit Design" , 2nd Edition, Wiley, 2008.
4. Christian Piguet, "Low-power CMOS circuits: technology, logic design and CAD tools", 1st Edition, Taylor & Francis Group, 2006.

Paper Code: MVD-603 **L T C**
Paper Title: ASIC Design **4 0 4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks :60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

Introduction to ASICs, CMOS Logic, ASIC library design, types of ASICs, design flow, CMOS transistors, CMOS design rules, Combinational logic cell, Sequential logic cell, Data path logic cell, Transistors as resistors, Transistor parasitic capacitance, Logical effort, Library cell design, Library architecture (10Hrs)

UNIT 2

Programmable Asics, logic cells and I/O cells, Anti fuse, static RAM, EPROM, EEPROM technology, PREP benchmarks, Actel ACT , Xilinx LCA, Altera FLEX, Altera MAX, DC & AC inputs and outputs, Clock & power inputs, Xilinx I/O blocks (10Hrs)

UNIT 3

Programmable ASIC Interconnect, design software and low level design entry, Actel ACT, Xilinx LCA, Xilinx EPLD, Altera MAX 5000 and 7000, Altera MAX 9000, Altera FLEX, design systems, Logic synthesis, Half gate ASIC, Schematic entry, Low level design language, PLA tools, EDIF, CFI design representation (10Hrs)

UNIT 4

ASIC construction, Floor planning, Placement and routing, system partition, FPGA partitioning, partitioning methods, floor planning, placement, physical design flow, global routing, detailed routing, special routing, circuit extraction, DRC (10Hrs)

References:

1. M.J.S Smith, "Application - Specific Integrated Circuits", 1st Edition, Addison Wesley Longman Inc., 1997.
2. Keith Barr, "ASIC Design in the Silicon Sandbox: A Complete Guide to Building Mixed-Signal Integrated Circuits", 1st Edition, McGraw Hill, 2008.
3. Himanshu Bhatnagar, "Advanced ASIC Chip Synthesis", 1st Edition, Kluwer Academic publishers, 2010.

Paper Code: MVD-605 **L T C**
Paper Title: VLSI Interconnects **4 0 4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks :60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

Introduction to VLSI interconnects, classification, Cu interconnection and dual damascene structure, stress void and electromigration phenomenon, Signal transmission on interconnects, On-chip interconnections, Package level interconnections (10Hrs)

UNIT 2

Analog VLSI Interconnects, physics of interconnects in VLSI, scaling of interconnects, Model for estimating wiring density, configurable architecture for prototyping analog circuits, Interconnect modeling, physical foundations for circuit models of interconnections, Loss and Lossless transmission line model, Optimum line model selection (10Hrs)

UNIT 3

Active and Passive interconnections, Multilevel and multilayer interconnections, Propagation delays, Crosstalk effects in digital circuits, spurious signals, crosstalk induced delay, energy dissipation due to crosstalk, crosstalk effects in logic VLSI circuits (10Hrs)

UNIT 4

Techniques for avoiding interconnection noise, noise detection problem, brief introduction to the testing of logic circuits, crosstalk-induced spurious signal detection, Introduction to optical and superconducting interconnects, basic parameters (10Hrs)

References:

1. Modeling and Simulation of High Speed VLSI Interconnects, A Special Issue of Analog Integrated Circuits and Signal Processing An International Journal, Vol. 5, No. 1, 1994.
2. Grabinski, Hartmut, "Interconnects in VLSI Design", 1st Edition, Springer, 2000.
3. Moll**,** Francesc, Roca**,** Miquel, "Interconnection Noise in VLSI Circuits", 1st Edition, Springer, 2004.

Paper Code: MVD-607	**L**	**T**	**C**
Paper Title: VLSI design Algorithms	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

VLSI automation algorithms, General graph theory and basic VLSI algorithms, Partitioning, problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms (10Hrs)

UNIT 2

Placement, floor planning & pin assignment, problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design, general & channel pin assignment (10Hrs)

UNIT 3

Global Routing, problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner tree based algorithms, ILP based approaches, problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms and switchbox routing algorithms (10Hrs)

UNIT 4

Over the cell routing & via minimization, two layers over the cell routers constrained & unconstrained via minimization, compaction, problem formulation, one-dimensional compaction, two dimension based compaction, hierarchical compaction (10Hrs)

References:

1. Sahib H.Gerez, "Algorithms for VLSI design automation", 1st Edition, John Wiley & Sons John Wiley & Sons, 1998.
2. Naveed Shervani, "Algorithms for VLSI physical design Automation", 2nd Edition, Kluwer Academic Publisher, 2005.
3. Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design",1st Edition, Kluwer Academic Publisher, 2002.
4. Rolf Drechsheler, "Evolutionary Algorithm for VLSI", 2nd Edition, 2002.

5. Trimburger," Introduction to CAD for VLSI",1st Edition, Kluwer Academic publisher, 2002.

Paper Code: MVD -609	**L**	**T**	**C**
Paper Title: VLSI Design Verification and Test	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

Introduction to digital VLSI Design flow, Design Representation, 3 Hardware Specific Transformations, Scheduling, Allocation and Binding, High level Synthesis, Verilog RTL Design, Combinational and Sequential Synthesis Logic Synthesis (10Hrs)

UNIT 2

Logic Optimization, Technology Mapping, Introduction to Hardware Verification and methodologies, Binary Decision Diagrams, construction, Reduction rules and Algorithms, Temporal Logic, Basic Operators, Syntax and Semantics of LTL, CTL and CLT (10Hrs)

UNIT 3

Equivalence and Expressive Power, Combinational equivalence checking, Introduction to verification, Modeling sequential systems, model checking algorithm, symbolic model checking, Automata and its use in Verification, Automata Theoretic Model Checking (10Hrs)

UNIT 4

VLSI Testing, Introduction, Test process, Test economics, Testing Defects, Errors, Fault models, Fault Simulation, Test generation for combinational circuits, Introduction to Automatic Test Pattern Generation, ATPG Algebras, Test generation algorithms for sequential circuits and Built in Self test. (10Hrs)

References:

1. D. D. Gajski, N. D. Dutt, A.C.-H. Wu and S.Y.-L. Lin, "High-Level Synthesis: Introduction to Chip and System Design", 1st Edition, Springer, 1992.
2. S. Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Prentice Hall, 2nd Edition, 2003.
3. G. De Micheli, "Synthesis and optimization of digital circuits", McGraw-Hill, 1st Edition, 1994.
4. M. Huth and M. Ryan, "Logic in Computer Science modeling and reasoning about systems", Cambridge University Press, 2nd Edition, 2004.

5. Bushnell and Agrawal, Essentials of Electronic Testing for Digital, Memory & Mixed-Signal Circuits, Kluwer Academic Publishers, Electronic series XVIII, 2000.

Paper Code: MVD -711	**L**	**T**	**C**
Paper Title: RF Integrated Circuits	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT 1

Introduction, RF systems, basic architectures, Maximum power transfer. Passive RLC Networks, Parallel RLC tank, Q, Series RLC networks, matching. Passive IC Components, Interconnects and skin effect, Resistors, capacitors, Inductors, review of MOS device physics (10Hrs)

UNIT 2

Distributed systems, Transmission lines, reflection coefficient, Lossy transmission lines, High frequency amplifier design, Noise, LNA design, Intrinsic MOS noise parameters, Power match versus noise match, Mixer design, Subsampling mixers (10Hrs)

UNIT 3

RF power amplifiers, classification of power amplifiers, Class A, AB, B, C amplifiers, Class D, E, F amplifiers, High efficiency power amplifiers, large signal impedance matching, Voltage controlled oscillators, Resonators, Negative resistance oscillators, Phase locked loops (10Hrs)

UNIT 4

Frequency synthesis and oscillators, Basic concepts, settling behavior, Frequency division, integer-N synthesis, Fractional frequency synthesis, design examples, Phase noise radio architectures, GSM radio architectures, CDMA, UMTS radio architectures (10Hrs)

References:

1. Thomas H. Lee., "The Design of CMOS Radio-Frequency Integrated Circuits" 2nd Edition, Cambridge University Press, 2006.
2. Behzad Razavi, "RF Microelectronics", 2nd Edition, Pearson, 2011.

Code No: MVD -613	**L**	**P**	**C**
Lab : Low power VLSI Design Lab	**-**	**2**	**1**

Experiments will be based on Low power VLSI Design Theory course

Code No: MVD -615	**L**	**P**	**C**
Lab : ASIC Design Lab	**-**	**2**	**1**

Experiments will be based on ASIC Design Theory course

Code No: MVD -617	**L**	**P**	**C**
Minor Project	**-**	**8**	**12**

Code No: MTVD -601	**L**	**P**	**C**
Dissertation	**-**	**30**	**24**

Code No: MTVD -603	**L**	**P**	**C**
Seminar and Progress Report	**-**	**4**	**4**